Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended): A method of fabricating an integrated circuit, the method comprising:

forming a barrier layer along lateral side walls and a bottom of a via aperture, the via aperture being configured to receive a via material that electrically connects a first conductive layer and a second conductive layer;

forming a seed layer proximate and conformal to the barrier layer; and

ion implanting elements into the seed layer, wherein the elements can be any one of Zn, Sn, Cr, Ca, Ag, and In, wherein ion implanting elements into the seed layer comprises low energy ion implanting elements into the seed layer, wherein low energy ion implanting comprises implanting at an energy of 2.0 KeV or less.

2. (Cancelled)

3. (Original) The method of claim 1, further comprising selectively controlling concentration of the implanted elements.

4. (Cancelled)

5. (Currently Amended) The method of claim 1, wherein the ion implanting is at a dosage concentration [an energy level] of IE15 to IE17 atoms/cm2.

6. (Original) The method of claim 1, further comprising tilting the integrated circuit thereby controlling placement of the implanted element on lateral side walls and the bottom of the via aperture.

7. (Currently Amended) The method of claim 1, [wherein the implanted element includes a copper (Cu) alloy] further comprising using a thermal process to facilitate mixing of implanted elements and the seed layer.

8. (Original): The method of claim 1, wherein the seed layer has a cross-sectional thickness of between 50 and 1,000 Angstroms.

9. (Original): The method of claim 1, wherein the seed layer is formed by an angle implant to achieve a uniform distribution of elements.

10. (Currently Amended): A method of implantation after copper seed deposition in an integrated circuit fabrication process, the method comprising:

providing a first conductive layer over an integrated circuit substrate;

providing a conformal layer at a bottom and sides of a via aperture positioned over the first conductive layer to form a barrier separating the via aperture from the first conductive layer;

providing an ultra-low energy ion implant of any one of Zn, Sn, Cr, Ca, Ag, and In to form a seed layer over the conformal layer, wherein ultra-low energy ion implant occurs at an energy level of 20.0 2.0 KeV or less;

filling the via aperture with a via material; and

providing a second conductive layer over the via material such that the via material electrically connects the first conductive layer to the second conductive layer.

11. (Original) The method of claim 10, wherein providing an ultra-low energy ion implant to form a seed layer over the conformal layer includes implanting a plurality of elements into the seed layer.

12. (Currently Amended) The method of claim 10, wherein providing an ultra-low energy ion implant to form a seed layer over the conformal layer includes providing an implant dosage concentration of IE15 to IE17 atoms/cm2.

13. (Original) The method of claim 10, wherein providing an ultra-low energy ion implant to form a seed layer over the conformal layer includes providing an implant depth of 50 to 1,000 Angstroms.

14. (Original) The method of claim 10, wherein the seed layer has a cross-sectional thickness of 50 to 1,000 Angstroms.

15. (Currently Amended) A method of forming a via in an integrated circuit, the method comprising:

depositing a first conductive layer;

depositing an etch stop layer over the first conductive layer;

depositing an insulating layer over the etch stop layer;

forming an aperture in the insulating layer and the etch stop layer;

providing a barrier material at a bottom and sides of the aperture to form a barrier layer;

providing a seed layer over the barrier layer;

providing a controlled low energy ion implantation of any one of Zn, Sn, Cr, Ca, Ag, and In into the seed layer, wherein low energy ion implantation comprises an energy level of 2.0 20.0 KeV or less;

filling the aperture with a via material.

16. (Original) The method of claim 15, wherein the ion implantation is at an angle of between 35 and 90°.

17. (Original) The method of claim 15, wherein control of ion implantation includes tilting the seed layer.

18. (Original) The method of claim 15, wherein the ion implantation into the seed layer includes B, P, or Ge elements.

19. (Original) The method of claim 15, wherein the barrier layer is Ta, TaN, or TiN.

20. (Cancelled)